MONT-BLANC

Newsletter December 2012

EUROPEAN APPROACH TOWARDS ENERGY EFFICIENT HIGH PERFORMANCE COMPUTING

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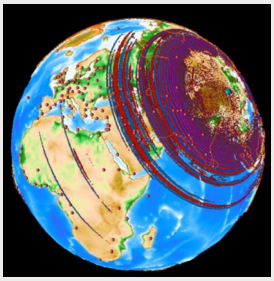

Early results of the porting of 11 real scientific applications on energy-efficient ARM based platforms

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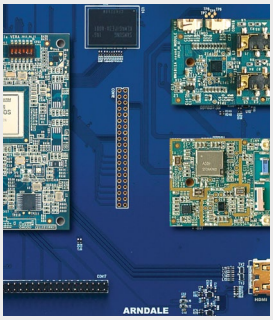

Mont-Blanc project selects Samsung Exynos 5 Processor

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Read full article

Mont-Blanc collaborates with...

DEEP Dynamical Exascale Entry Platform

DEEP is an innovative European response to the Exascale challenge. The DEEP consortium will develop a novel, Exascale-enabling supercomputing architecture with a matching SW stack and a set of optimized grand-challenge simulation applications.

DEEP takes the concept of compute acceleration to a new level: instead of adding accelerator cards to Cluster nodes, an accelerator Cluster, called Booster, will complement a conventional HPC system and increase its compute performance. Together with a software stack focused on meeting Exascale requirements, comprising adapted programming models, libraries and performance tools, the DEEP architecture, will enable unprecedented scalability.

www.deep-project.eu

Message from the coordinator

Welcome to the second edition of the Mont-Blanc newsletter!

Now the project has been operating for one full year already, and there is quite a bit that we have accomplished in that time: we have selected an ARM-based SoC and defined the Mont-Blanc system architecture, deployed a full HPC software stack, and ported a number of full-size applications to ARM.

Further to the recently announced SoC selection, we have also developed the FORTRAN support for the OmpSs parallel programming model, and deployed a full HPC system software stack on the ARM platform. Now, HPC developers face a familiar environment with OS, compilers, scientific libraries, runtime system, cluster management, performance analysis tools and parallel debugger that makes applications porting to ARM not harder than porting to any other HPC system. All of our 11 starting applications have been successfully ported and tested on our test ARM multicore cluster.

During the next year 2013 we will be developing the first Mont-Blanc prototype hardware: a cluster-on-a-blade architecture, integrated into a standard BullX chassis, with an integrated Gnodal high bandwidth Ethernet interconnection network. In parallel with the hardware development, we will develop the required OpenCL support for the embedded GPU in the HPC system software stack, starting from the OpenCL runtime environment itself, the OmpSs runtime library, and the scientific libraries. Finally, we will start porting the applications to the OmpSs tasking model, focusing on their task partitioning and scalability to higher number of low-power compute nodes to ensure competitive performance on our platform.

The project continues to draw significant interest from the community as ARM-based server SoC and systems continue to be announced, so we face the additional responsibility to keep up with the expectations we have created. We will not disappoint you. Please stay tuned for more in the next editions of our newsletter. You can also follow us via web, Facebook or Twitter!

Alex Ramírez
Mont-Blanc Coordinator

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During the session, Prof. Ramirez announced the selection of the Samsung Exynos platform as the building block for powering Mont-Blanc's first integrated low power High Performance Computing (HPC) prototype. This session was organized in collaboration with other EU- funded Exascale initiatives such as DEEP and CRESTA.

In parallel, Mont-Blanc also presented a session entitled "Energy Efficient HPC" at the BoF with more than 60 participants in the room, headed by Simon McIntosh-Smith from the University of Bristol. This second edition of EEHPC session included 5 minute talks from the experts in this field, followed by an open panel session where the audience put questions to the speakers.

Image: Alex Ramirez, Mont-Blanc coordinator, during SC12

In the exhibition hall, the project was represented in different partner booths such as the ones from the Barcelona Supercomputing Center, Bull, ARM, Gnodal and Juelich Forschungszentrum. A lot of visitors got interested about the announcement during the conference about the selection of the processor for the future prototype.

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Another highlight was the presentation of a short video that gives an overview about the project and why energy efficiency is already a primary concern for the design of any computer system. It is unanimously recognized that future Exascale systems will be strongly constrained by their power consumption.

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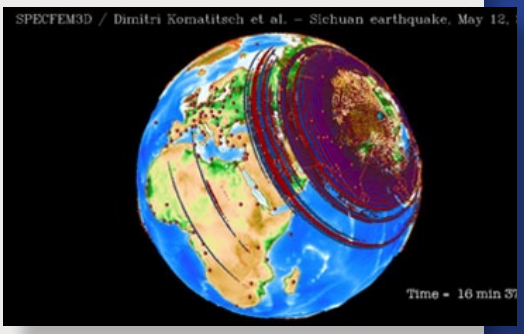
Early results of the porting of 11 real scientific applications on energy-efficient ARM based platforms

One of the three major goals of the Mont-Blanc project is to assess the behaviour and the programmability of future Multi-Petascale and Exascale ARM-based low-power clusters on up to 11 scientific applications. Considering that five to ten years are necessary to design, develop and validate a new generation of scientific applications, it is mandatory to anticipate upcoming architectural Exascale breakthroughs in order for the European HPC centres to prepare scientists to adapt or develop new applications with fitted programming models and stay at the forefront of their disciplines.



SPECFEM3D simulation of the Sichuan earthquake

The eleven real applications, used by academia and industry, are in daily production on existing European (PRACE Tier-0 systems) or national HPC facilities. They were selected by the project partners in order to cover a wide range of scientific domains (including geophysics, fusion, materials, particle physics, life sciences, combustion, and weather forecast) as well as hardware and software needs.

During the first year of the Mont-Blanc project, the project consortium members managed to port all 11 applications to the first hardware platforms available, and to perform an initial performance and power consumption profiling of almost all of them.

The initial porting of the applications was done by using the standard GNU tool chain as well as numerical, I/O and parallel libraries compiled and made available by the project. This shows that the current software environment is stable enough for porting such complex applications into current ARM-based systems. SPECFEM3D is a good example to highlight from this initial phase. It is an established Petascale-proven production code, written in Fortran95 with 80 000 lines of code, used to simulate three-dimensional seismic wave propagation in the whole Earth following earthquakes. The effective use of an application like this has a strong societal impact by making it possible to forecast aftershocks following major earthquakes and providing civil authorities with important information for moving civilians to safety.

After porting and performing specific ARM compiler optimisations, it was possible to scale SPECFEM3D out with a very good strong scaling on up to 192 cores of the Tibidabo cluster (based on 96 Tegra2 boards where each has a dual core ARM A9 socket interconnected by regular Gigabit Ethernet switches). Since Tibidabo is not a performance oriented platform and was designed more for initial porting/profiling of the applications and assessment of the software stack, an average gap of 10x lower performance then on regular x86 cluster was observed on almost all the applications. However a 4x better energy-efficiency between Tibidabo and a regular x86 cluster was also observed.

The in-depth profiling exercise allowed pertinent fractions exhibiting specific computational or communication patterns, called kernels, to be extracted from real applications. These kernels will be re-coded using OmpSs, a task based programming model capable of hiding the underlying complex hardware of future systems from the programmer.

After the selection of the Samsung Exynos Dual platform as the hybrid building block for powering its first integrated low-power high-performance prototype, the next phase of the project will be devoted to selecting a subset of fitted hybrid applications and to performing specific porting and optimisation. This incremental co-design effort of porting legacy applications, extracting and re-coding kernels using OmpSs, backporting the final result into original applications and sharing best-practises, will help to evaluate the time-to-solution needed on application development for using embedded accelerated components targeted for future Exascale systems.

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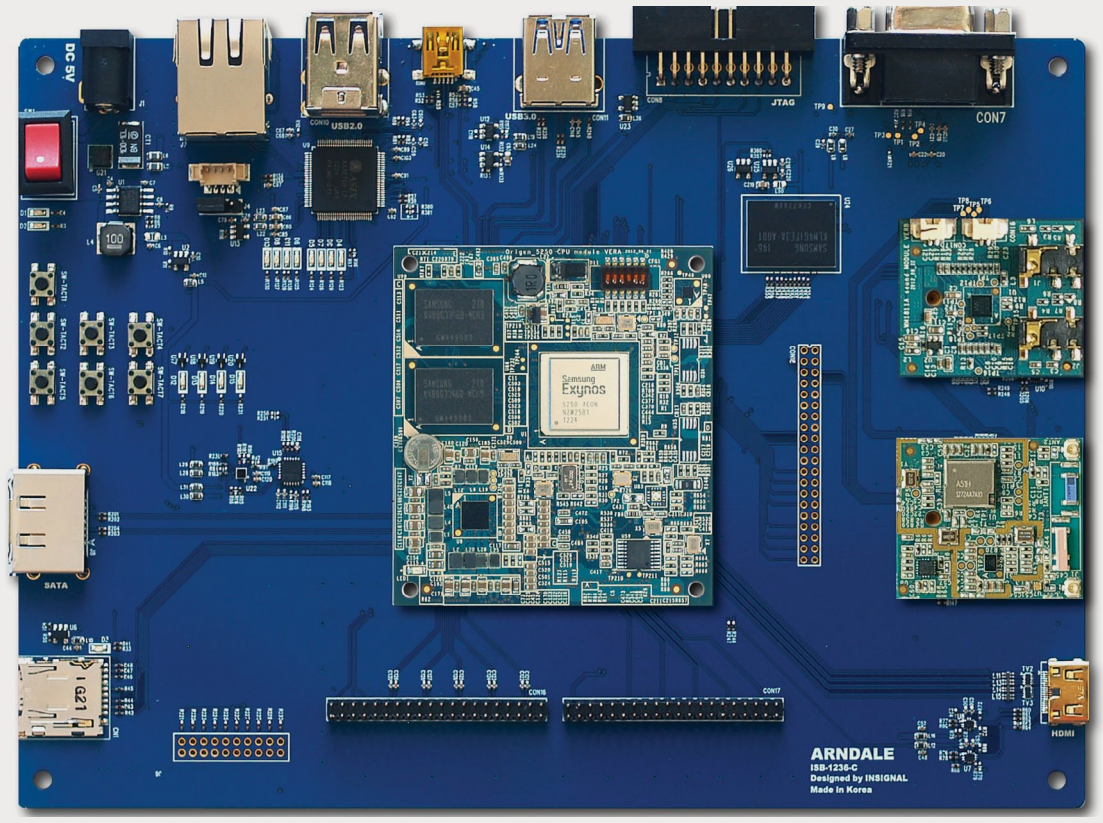
The Samsung Exynos 5 Dual is built on 32nm low-power HKMG (High-K Metal Gate), and features a dual-core 1.7GHz mobile CPU built on ARM® Cortex™-A15 architecture plus an integrated ARM Mali™-T604 GPU for increased performance density and energy efficiency. It has been featured and market proven in consumer and mobile devices such as Samsung Chromebook and Google's Nexus 10.

This will be the first use of an embedded mobile SoC in HPC, which enables the Mont-Blanc project to explore the challenges and benefits of deeply integrated energy-efficient processors and GPU accelerators, compared to traditional homogeneous multicore systems, and heterogeneous CPU + external GPU architectures.

"The Exynos 5 Dual packs the most powerful ARM processors with a programmable GPU in a low-power mobile device that would normally be in someone's pocket and running on a battery. Its performance density, energy efficiency, and low market price make it an extraordinary building block for prototyping a new generation of HPC systems." says Alex Ramirez, coordinator of the Mont-Blanc project.

During the first year of activities, Mont-Blanc has focused on deploying successfully an HPC system software stack and full-scale scientific applications on ARM platforms, proving that ARM-based architectures are feasible alternatives for HPC. Now the efforts gear towards integration of the Exynos platform on a HPC solution, and software exploitation of the embedded GPU.



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