European Program to Develop Supercomputing Chips Begins to Take Shape

Michael Feldman (/project/top500-news-team/) | July 5, 2018 22:27 CEST

The European Processor Initiative (EPI), an ambitious program to develop a pair of chips for domestic supercomputers, is poised to change the way Europe does HPC. And although the work is still very much in its early stages, it looks like the Europeans have selected their preferred processor architectures: Arm and RISC-V.

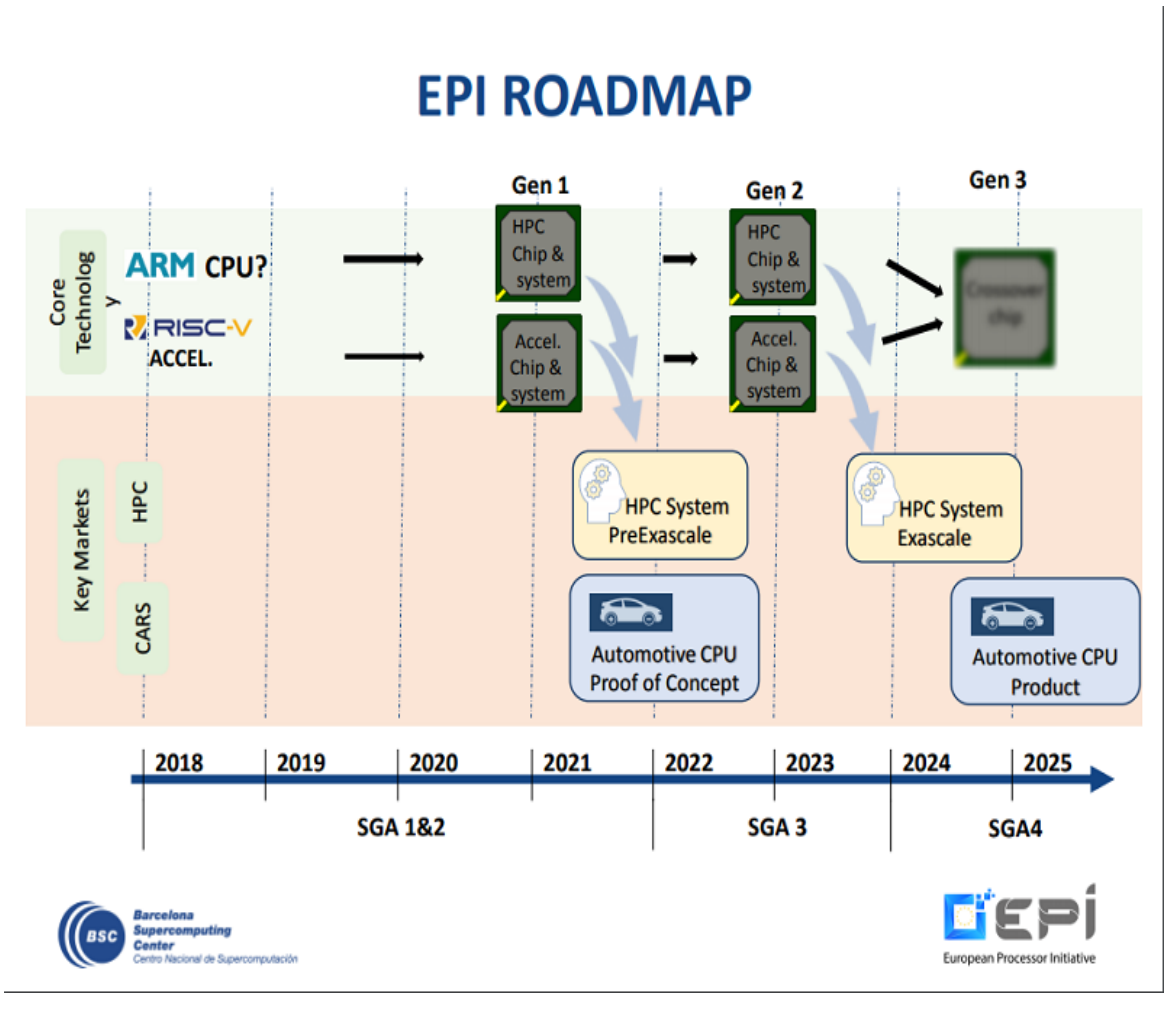
Launched in March 2018 (https://ec.europa.eu/digital-single-market/en/news/european-processor-initiative-consortium-develop-europes-microprocessors-future-supercomputers) by the European Commission, the EPI's overall aim is to develop domestically produced low-power microprocessors for the European market. Even though the work is focused on delivering chips for HPC, and in particular for exascale supercomputers, the technology will also be applied to the broader datacenter market, as well as the automotive industry. The rationale for this more expansive strategy is provide higher volume markets that can economically sustain the considerable effort involved in chip R&D and support..

The first generation of these HPC processors are expected to be delivered toward the end of the decade, in time to form the basis for pre-exascale supercomputers scheduled to be deployed across the EU in the 2020 to 2021 timeframe. The second-generation chips will power Europe's first exascale systems in 2023 and 2024. The system work is being led by EuroHPC, a group formed to bring Europe on par with the US, China, and Japan in high performance computing technology. Part of the mission involves developing home-grown componentry so that EU members have more control over what goes into their supercomputers.

The most central element of these systems is the processor, which puts EPI in the critical path for the EuroHPC work. In a statement delivered at the launch of EPI in March, Vice-President Andrus Ansip, who heads the Digital Single Market, and Mariya Gabriel, the Commissioner for Digital Economy and Society, summed up the strategy as follows:

"The European Processor Initiative is an important step of a strategic plan to develop an independent and innovative European supercomputing and data ecosystem and will ensure that the key competence of high-end chip design remains in Europe, a critical point for many application areas. Thanks to such new European technologies, European scientists and industry will be able to access exceptional levels of energy-efficient computing performance. This will benefit Europe's scientific leadership, industrial competitiveness, engineering skills and know-how and the society as whole."

The program will develop two types of processors: one for general-purpose HPC processing, the other for throughput acceleration. By the looks of it, an Arm design will the basis for the former, while RISC-V will provide the architecture for the latter. A presentation (https://content.riscv.org/wp-content/uploads/2018/05/11.15-11.45-EXASCALE-RISC-V-Mateo.Valero-9-5-2018-1.pdf) delivered by Barcelona Supercomputing Centre (BSC) director Mateo Valero in May, reflected some of the current thinking on this strategy, including the roadmap for chip development, as illustrated below.



Source: RISC-V Workshop presention from Prof. Mateo Valero (https://content.riscv.org/wp-content/uploads/2018/05/11.15-11.45-EXASCALE-RISC-V-Mateo.Valero-9-5-2018-1.pdf), May 9, 2018,

The choice of Arm certainly makes sense, given its European roots in the UK, and its commercial licensing scheme. Anyone can buy an Arm license and develop a processor of their own design, something not possible with Intel, AMD, or NVIDIA technology. In some ways, RISC-V is even more attractive, since it's offered as an open standard architecture that can be had at no cost under a BSD license, either for developing free implementations or proprietary designs.

It's worth noting that the selection of Arm and RISC-V has not been officially announced. However, given inclination of some of the major European players — the long history of the Mont-Blanc exascale project with Arm (including its latest project to build an Arm-based SoC for exascale machines (/news/mont-blanc-2020-project-sets-sights-on-exascale-processor/)), BSC's enthusiasm for RISC-V (it recently hosted the RISC-V Workshop (https://tmt.knect365.com/risc-v-workshop-barcelona/)), and Atos's interest in both architectures (http://montblanc-project.eu/wp-content/uploads/2018/03/20180208_Primeur_The-European-Processor-Initiative-EPI-to-develop-the-processor-that-will-be-a.pdf) — it's hard to fathom any other choice. Of course, OpenPower and even MIPS are possibilities, but neither one has been the focus of any European HPC research. Coming up with a completely new processor architecture is the least likely option, given the timeframes for the pre-exascale and exascale deployments.

There's a good chance the EPI Arm implementation for HPC will be based on the SVE (Scalable Vector Extensions) variant of the architecture, which is the same one that Fujitsu is using to develop the processor that will power RIKEN's Post-K exascale supercomputer. If some of the Japanese work, especially the system software and tools development, could be reused for the EPI project, a lot of effort could be saved.

The development of the RISC-V accelerator is going to entail a good deal more work, if only for fact that there are no examples of high-end designs to draw upon. RISC-V is of recent vintage, having been introduced at the University of California, Berkeley in 2010. Its vector capability is somewhat lacking for an HPC architecture, although at the previously mentioned RISC-V workshop, a 128-bit vector extension was discussed. The fact that RISC-V is being used as high-throughput accelerator could simplify the design effort to some extent since there it wouldn't have to incorporate all the control flow logic expected in a general-purpose processor.

Up until this year, the development of these domestic chips could be considered something of an exercise in isolationism or perhaps even vanity. The multinational nature of the semiconductor industry doesn't limit European access to the latest technology from US or anywhere else. But with a trade war now being instigated by the current administration in Washington, even computer chips could soon run into tariffs on their journey through the global supply chain. If that turns out to be the case, the EU decision to develop a home-grown chip capability would have been prescient.

The EU has initially invested €120 million toward the EPI program, but the 23 industry and research partners are expected to kick in a certain amount as well. The key players include Atos, BSC, CEA, Jülich Supercomputing Centre, and STMicroelectronics, to name a few. BSC has taken the lead for the accelerator work, while Atos has taken on the role of system/chip integrator for the general-purpose processor. Work on both designs was supposed to begin mid-year, so we can assume that the development effort is now underway.

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