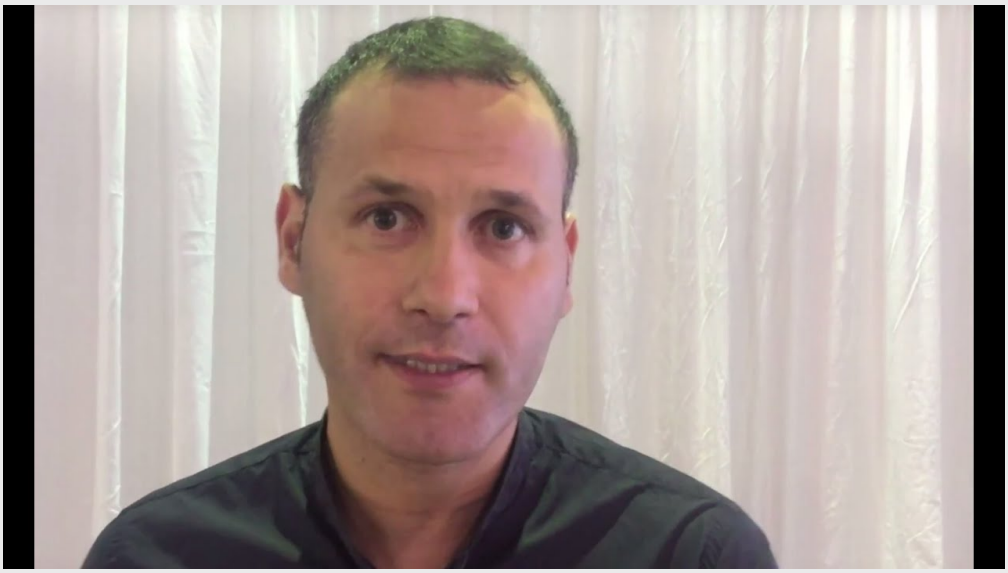
Primeur Weekly! Magazine

Mont-Blanc 2020 project to develop key building blocks for the European Processor Initiative



18 Oct 2018 Frankfurt - *At the ISC'18 Conference in Frankfurt, Germany,Primeur Magazinemet Said Derradji, project coordinator of the Mont-Blanc 2020 project, on the Exhibition floor. Said Derradji works at Atos R&D in the Big Data and Security Department. The Mont-Blanc project has always been a pioneer in ARM for HPC. The first Mont-Blanc project was using a mobile processor to do HPC. The following projects, Mont-Blanc 2 and Mont-Blanc 3, focused on the ARM ecosystem and software ecosystem. Mont-Blanc 3 built a real platform with a several-grade ARM CPU, the Cavium ThunderX2. Mont-Blanc 2020 is the sequel of the Mont-Blanc project story. The idea is to now be able to develop a System-on-Chip (SoC), a European processor, based on ARM cores and optimized for HPC.*

The main driver is memory bandwidth: What will be the best way to use the new instruction set from ARM Scalable Vector Extension (SVE), the vector lengths and the memory bandwidth, a revolution that the team can achieve with HPM technology? The objective of Mont-Blanc is to start developing building blocks (IPs). The team will develop ASIC modules and be able to demonstrate on an emulator. The team will not build ASIC in the scope of this project but it will develop the same ASIC flow as it does for ASIC in Atos. This IP will be reused and productized for the European Processor Initiative (EPI) that will rely on the work done in the Mont-Blanc 2020 project.

Primeur Magazine: What exactly do you mean by processor?

*Said Derradji:*The team will build a complete SoC but the core will come from ARM. In the proposal, one focuses on the Network-on-Chip (NoC) and the memory controller, all the infrastructure that ensures that the team can optimize and fully utilize the vector units with this memory bandwidth because having this huge compute capacity without being able to fill these units with the necessary memory bandwidth is one of the challenges that the team wants to address. The NoC is an essential part of the SoC. It is a key IP for the project team to master all the components to be able to build a different variety of SoCs to address other markets. A new target in Mont-Blanc is to look at a different market than HPC to be able to have an economical sustainability. In Mont-Blanc 2020, the team will look with a new partner which is Kalray, to the automotive market for autonomous driving applications. The partners will look at an automotive interface with accelerators for the automotive market and HPC. The first market that seems natural is embedded HPC in autonomous driving vehicles.

Primeur Magazine: In Japan, Fujitsu is also developing a processor based on ARM for HPC. Are you working with them?

*Said Derradji:*Actually, the Mont-Blanc 2020 team is partnering with RIKEN, which will be the user of the Fujitsu CPU, and they are sharing a model to be able to port an application already and using SVE compilers. The Mont-Blanc 2020 team is working with them because the ecosystem for HPC, and most importantly for SVE, is new and it must be demonstrated on real applications. The team is working with them on models of the SVE and also of the compiler and the library associated to it. So, Mont-Blanc 2020 is working closely with RIKEN, not on the real SoC design but on the software ecosystem.

Primeur Magazine: You are also closely working with ARM?

*Said Derradji:*Yes. One important goal of the project is to have real performance and return on investment (ROI) and power cost of the SVE. The team will work with ARM and ARM will provide in 7 nanometer technology what will be the power cost, the max frequency and the silicon area that will be necessary for building the SoC.

Primeur Magazine: ARM is also one of the partners?

*Said Derradji:*Yes, ARM is an important and very active partner for this project. There is a reduced set of partners for this Mont-Blanc 2020 project compared to the previous projects and also for the EPI project. There is ARM, Kalray for the automotive part, Jülich Supercomputing Centre as a user, CEA as a user but also as a technology provider because they are experts in interposing for HPM. One has to build an interposer for die to die connection and CEA is an expert in that area. ARM has provided the core. Atos is the integrator and is also designing IPs for the network concept. There is also the Barcelona Supercomputing Centre (BSC), the founding member of the Mont-Blanc project and the coordinator of the first Mont-Blanc project, and a small start-up, SemiDynamics, a Spanish company, that will work on the HPM memory controller.

The idea is to provide special features for the HPM controller and to take the opportunity to implement optimization across all the IPs made in the project, and not buy an IP from an external provider, and bridging them to be able to build the full pass. The idea is that when you build your IP, you are able to optimize features for the whole chip. For HPC design, you have to do it this way. SoC integration is something common but HPC is very sensitive in terms of latency, work performance, prefetched optimization, and software interface. There is a lot of co-design with Jülich, BSC, and CEA. The team is able to implement specific features in the IPs from the SVE compute unit to the memory. It includes the memory controller, the Network-on-Chip, and the coherence protocol that will be customized for this project.

Primeur Magazine: Using the experience of the previous projects, the Mont-Blanc 2020 project is focused on creating something that after this project can be really used and applied?

*Said Derradji:*Exactly. During the previous project, Mont-Blanc 3, there was some architectural exploration of what could be an ARM-based node for HPC. This project is more focused on implementing. The team will perform IP design and ASIC design. There is an ASIC design team within Atos and SemiDynamics, that will do real coding and physical implementation on 7 nanometers. The team will not go to production, obviously due to the cost. This is part of another initiative that will be coming afterwards with more funding. Mont-Blanc 2020 will demonstrate the technology on an emulator. Therefore, you need a level of IP that is very advanced. You have to synthesize it. It will not be a model, it will be a real design, put on an emulator, based on FPGA. The only difference will be the speed because FPGA will run slow on a real design but in terms of constraints for the designer, it will be almost at production level.

Primeur Magazine: Because you are so close to production, this means that it is also important for each part of the design who owns the intellectual property right. Do you have a consortium agreement where this is settled?

*Said Derradji:*Yes. There is a consortium agreement for the IP stating that all the partners will be able to use the IP but the designer of the IP, the provider, will keep the right for the IP. It is not a real issue because with regard to the European Processor Initiative that obviously will use this IP, all the partners of this project are also partners of the European Processor Initiative. There is a good team of partners. In terms of co-design, there is Jülich, CEA and BSC. For software, there is ARM which for the Mont-Blanc platform puts a lot of effort in the HPC ecosystem including libraries and tools. There is an ASIC design team consisting of SemiDynamics, Atos and BSC for some part. The consortium has the full range of skills to discuss and design a real product, going from modelling which was the initial work on the Mont-Blanc architecture exploration, to design and most importantly validation. Now, in ASIC design, the most important effort is no longer design but the verification. This is the key for this project.

It is not a huge project in terms of funding but the focus is on IPs that the partners think are critical for the performance of the design. The driver of the project is memory bandwidth and optimization with the SVE compute unit because there are some parameters in play including the width of the vector units which is something that can be modified. The beauty of SVE is that it is agnostic for vector lengths. The HPM bandwidth is something new. Are the partners able to use this huge amount of bandwidth efficiently? The partners' vision is that the Network-on-Chip will be key for that, the wires, but also the coherence protocol and the way the design is partitioned. There is room for a lot of innovation in that part.

Primeur Magazine: Just some numbers. What is the size of the project?

*Said Derradji:*It is a 7 million euro project. Most of the effort will be on the IP design. There is some application porting. At the beginning of the project, the partners have selected some applications. With the experience of the previous Mont-Blanc projects, this has been very easy and did not cost a lot of effort. ARM is providing the models. There is a shared effort with the Mont-Blanc 3 project. The main effort will be on the ASIC and IP design. The emulator is also a

very costly tool that will be provided by CEA. They have an emulator and will rent it to the partners for some time at the end of the project. In terms of funding, it is not big for such an ambitious project but all the resources will be focused on optimizing the critical elements. The real funding for making the processor will come afterwards with the European Processor Initiative.

Primeur Magazine: When will the Mont-Blanc 2020 project finish?

*Said Derradji:*The Mont-Blanc 2020 project will finish in two years because it has started already one year ago. The partners have synchronization and milestones that are coming in synchronization with EPI before the end of the project. The partners will have parallel development phases with EPI. The workflow from application to demonstration on the emulator will be finishing in two years now.

Primeur Magazine: Thank you very much for this interview.

Ad Emmen

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